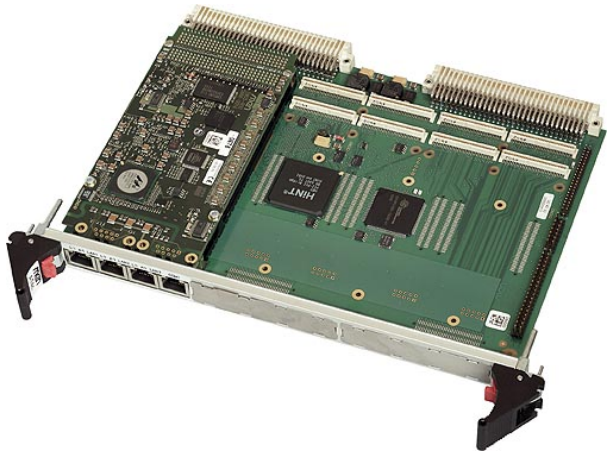
Embedded Solutions

A14C - 6U VME64 MPC8540 SBC / PMC



- **PowerPC® MPC8540 / 800MHz**
- **FPGA 12,000 LEs (approx.144,000 gates)**
- **1-slot 64-bit VMEbus master and slave**
- **Up to 2 GB (ECC) DRAM**
- **NAND Flash, FRAM**
- **Graphics via PMC or FPGA**
- **2 Gigabit/1 Fast Ethernet**
- **Up to 6 COMs**
- **Parallel ATA for onboard hard disk**
- **Further I/O individually via FPGA**
- **2 PMC slots**
- **MENMON™ BIOS for PowerPC® cards**

The A14C is an advanced PowerPC® based single-board computer for embedded applications. It features full VME64 support and it can be used as a master or a slave in a VMEbus environment. The A14C provides 1 MB local shared SRAM for slave access and communication between the local CPU and another VMEbus master.

The A14C is controlled by an MPC8540 integrated PowerPC® processor working at 800MHz. The SBC is equipped with a DDR SO-DIMM socket for data storage, with NAND Flash for program storage as well as with non-volatile FRAM. The board provides front-panel access for two Gigabit Ethernet, one fast Ethernet and one COM via four RJ45 connectors. Four more UARTs are optionally accessible via SA-Adapters™ for front connection.

Additional functionality such as graphics, touch, CAN, binary I/O etc. can be realized as IP cores in FPGA for the needs of the individual application. The corresponding PHYs are available via SA-Adapters™ on a transition module to the rear.

The FPGA acts as a standard PCI device on the A14C. The FPGA functions are loaded by software during power-up within less than 1s. FPGA updates can be carried out dynamically during operation.

In addition, the A14C can be equipped with PMC mezzanine cards supporting 64 bits/66 MHz as well as front I/O and rear I/O (PIM).

The A14C comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

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Technical Data

CPU
- PowerPC®
  - MPC8540 PowerQUICC™ III
  - 800MHz (666..833MHz optional)
  - e500 PowerPC® core with SPE APU and MMU
  - Integrated Northbridge and Southbridge
  - High memory bandwidth

Memory
- 2x32KB L1 data and instruction cache, 256KB L2 cache / SRAM integrated in MPC8540
- Up to 2GB SDRAM system memory
  - SO-DIMM slot for SDRAM modules
  - DDR2100 with or without ECC
  - 133MHz memory bus frequency
- Up to 1GB soldered NAND Flash (and more), FPGA-controlled
- Up to 16MB additional SDRAM, FPGA-controlled, e.g. for video data and NAND Flash firmware
- 8MB boot Flash
- 32KB non-volatile FRAM
- Serial EEPROM 4kbits for factory settings

Mass Storage
- Parallel IDE (PATA)
  - One port for hard-disk drives
  - Drive can be connected via ribbon cable or mounted directly on the CPU board using MEN adapter kit (instead of PMC modules)
  - Only one VMEbus slot needed even with hard disk
  - PIO mode 0 support
- Up to 1GB soldered ATA NAND Flash (and more), FPGA-controlled

I/O
- Three Ethernet channels
  - Two 10/100/1000Base-T Ethernet channels
  - One 10/100Base-T Ethernet channel
  - Three RJ45 connectors at front panel
  - Two onboard LEDs to signal LAN Link and Activity
- One RS232 UART (COM1)
  - One RJ45 connector at front panel
  - Data rates up to 115.2kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS
- One LVTTL UART (COM10)
  - FPGA-controlled
  - Accessible via rear I/O
  - Data rates up to 115.2kbits/s
  - 60-byte transmit/receive buffers
  - Handshake lines: CTS, RTS; DCD, DSR, DTR; RI
- Quad UART (COM20..COM23)
  - Physical interface using SA-Adapters™ via 10-pin ribbon cable on I/O connector
  - RS232..RS485, isolated or not: for free use in system (e. g. cable to front)
  - Data rates up to 115.2kbits/s
  - 128-byte transmit/receive buffer
  - Handshake lines: CTS, RTS; DCD, DSR, DTR; RI
- GPIO
  - 39 GPIO lines
  - FPGA-controlled
  - Accessible via rear I/O

Front Connections
- Three Ethernet (RJ45)
- COM1 (RJ45)
- COM20..COM23 (optional, instead of PMC modules, or in second front-panel slot)
- PMC 0 and 1

Rear I/O
- COM10
- GPIO
- Mezzanine rear I/O: PMC 0

FPGA
- Standard factory FPGA configuration:
  - Main bus interface
  - 16Z070_IDEDISK - IDE controller for NAND Flash
  - 16Z043_SDRAM - Additional SDRAM controller (16MB)
  - 16Z023_IDENHS - IDE controller (PIO mode 0; non-hot-swap)
  - 16Z025_UART - UART controller (controls COM10)
  - 16Z034_GPIO - GPIO controller (40 lines, 5 IP cores)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

Mezzanine Slots
- Two PMC slots
  - Compliant with PMC standard IEEE 1386.1
  - Up to 64-bit/64-MHz, 3.3V V(I/O)
  - PMC I/O module (PIM) support through J4

Miscellaneous
- Real-time clock with GoldCap backup
- Power supervision and watchdog
- Reset button, GPIO-controlled, in ejector handle

Local PCI Bus
- 32-bit/33-MHz, 3.3V V(I/O)
- Compliant with PCI Specification 2.2

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Technical Data

VMEbus
- Compliant with VME64 Specification
- Slot-1 function with auto-detection
- Master
  - D08(EO):D16:D32:D64:A16:A24:A32:ADO:BLT:RMW
- Slave
  - D08(EO):D16:D32:D64:A16:A24:A32:BLT:RMW
- 1MB shared fast SRAM
- DMA
- Mailbox functionality
- Interrupter D08(O):I(7-1):ROAK
- Interrupt handler D08(O):IH(7-1)
- Single level 3 fair requester
- Single level 3 arbiter
- Bus timer
- Location Monitor
- Performance
  - Coupled read/write D32 non-block transfer rate 6.5 MB/s
  - DMA read/write D32 BLT transfer rate 12.1 MB/s
  - DMA read/write D64 MBLT transfer rate 25 MB/s

Electrical Specifications
- Supply voltage/power consumption:
  - +5V (-3%/+5%), 3A typ.
  - +12V (-5%/+5%), only provided for PMCs that need 12V
  - -12V (-5%/+5%), only provided for PMCs that need 12V
- MTBF: 92,800h @ 40°C (derived from MIL-HDBK-217F)

Mechanical Specifications
- Dimensions: standard double Eurocard, 233.3mm x 160mm
- Weight (without PMC modules): 450g

Environmental Specifications
- Temperature range (operation):
  - 0..+60°C
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

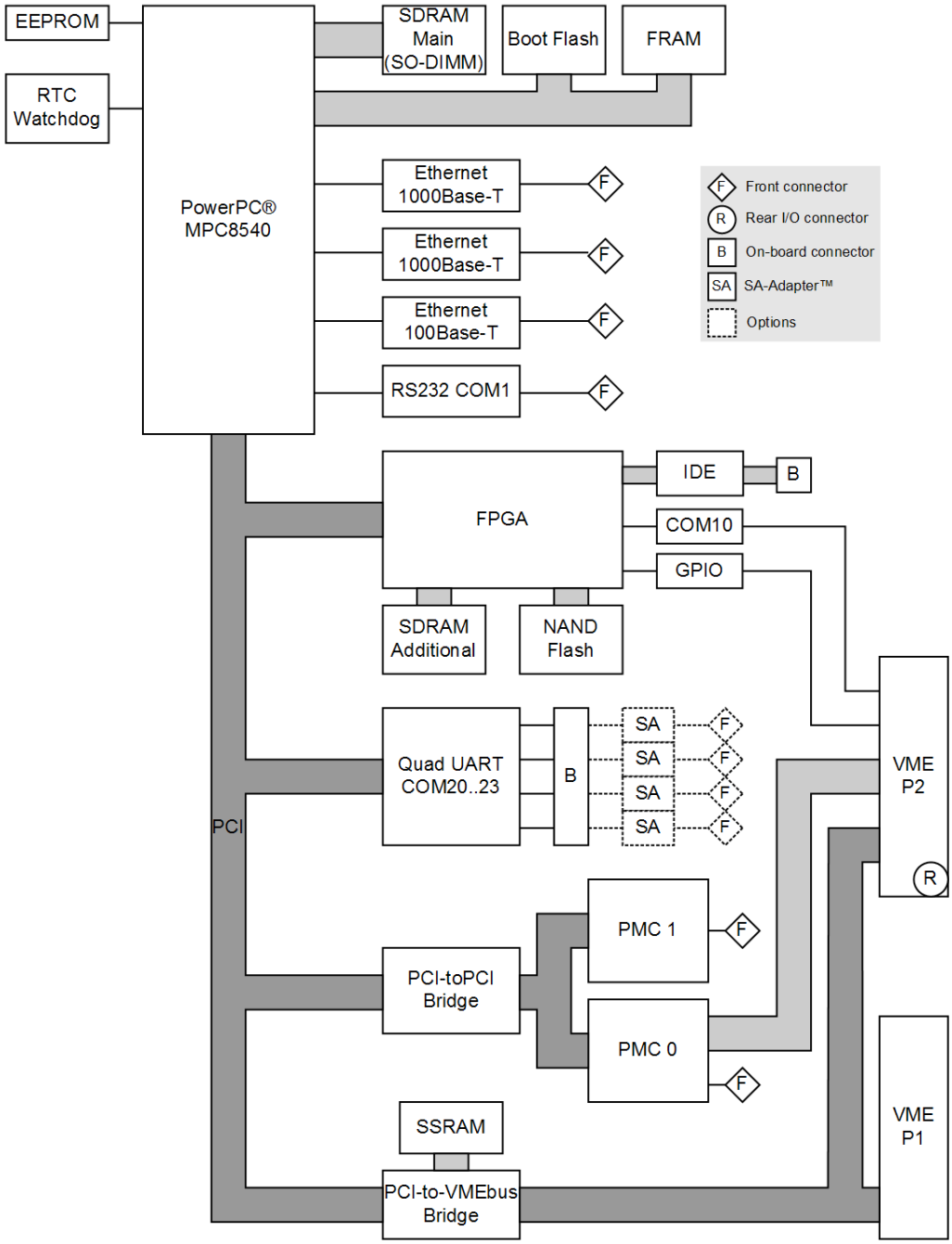
Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

BIOS
- MENMON™

Software Support
- VxWorks®
- Linux (ELinOS)
- QNX®
- For more information on supported operating system versions and drivers see Software.

Diagram


EEPROM
RTC
Watchdog
PowerPC®
MPC8540
SDRAM
Main
(SO-DIMM)
Boot Flash
FRAM
Ethernet
1000Base-T
Ethernet
1000Base-T
Ethernet
100Base-T
RS232 COM1
F
Front connector
R
Rear I/O connector
B
On-board connector
SA
SA-Adapter™
Options
FPGA
IDE
COM10
GPIO
SDRAM
Additional
NAND
Flash
Quad UART
COM20..23
SA
PCI
VME
P2
PMC 1
PMC 0
PCI-toPCI
Bridge
SSRAM
PCI-to-VMEbus
Bridge
VME
P1

Configuration & Options

Standard Configurations

Article No.	CPU Type	Clock	System RAM	NAND Flash	Additional SDRAM	FRAM	Boot Flash	Mezzanine Slots	Operation Temperature
01A014C00	MPC8540	800 MHz	512 MB (no ECC)	128 MB	16 MB	32 KB	8 MB	2 PMC	0..+60°C

Options

CPU

- Type
  - MPC8540
  - MPC8560
- Clock
  - 666..833 MHz

Memory

- System RAM
  - 256 MB, 512 MB, 1 GB or 2 GB
  - With or without ECC
- NAND Flash
  - 0 MB up to maximum available
- Additional SDRAM
  - 0 MB or 16 MB
- FRAM
  - 0 MB or 32 MB
- Boot Flash
  - 8 MB or 16 MB

I/O

- Quad UART (COM20..23)
  - Direct onboard connection via 10-pin connectors, instead of PMCs
- Front Connections
  - D-Sub instead of RJ45 connectors

Mezzanine Slots

- 2 PMC
- 3 PC-MIP®

Operation Temperature

- 0..+60°C

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® EP1C12
  - 12,060 logic elements
  - 239,616 total RAM bits
- Connection
  - Available pin count: 47 pins
  - Functions available via onboard and rear I/O connectors

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Ordering Information

Standard Hardware

01A014C00	MPC8540/800MHz, 512MB DRAM, 128MB NAND Flash, 16MB graphics memory, 32KB FRAM, 2 PMC slots, 0..+60°C

SA-Adapters

05A013-00	Mounting kit for 4 SA-Adapters for 6U VME/cPCI boards, incl. 1-slot front panel and ribbon cable, without SA-Adapters
08SA01-00	RS232, not optically isolated, 0..+60°C
08SA02-00	RS422/485, half duplex, optically isolated, 0..+60°C
08SA02-01	RS422/485, full duplex, optically isolated, 0..+60°C
08SA02-07	RS422/485, full duplex, optically isolated, -40..+85°C screened
08SA03-00	RS232, optically isolated, 0..+60°C
08SA03-01	RS232, optically isolated, -40..+85°C screened

Systems & Card Cages

Miscellaneous

05F006-00	RS232 interface cable RJ45 to 9-pin D-Sub (1 COM to 1 COM), 2m
0710-0028	Industrial PATA hard disk, 2.5", 80GB, 24hours/7days, for on-board mounting (hard disk mounting kit may be required additionally), -30..+85°C qualified
08AD71-00	AD71, 2.5" hard disk adapter for A13, A14, A15, D6, D7

Software: OS independent

13Z017-06	MDIS5 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

13Z014-90	Linux device driver (MEN) for PCI-to-VME bridge on A12, A13, A14, A15, A17, A19, A20 and B11
13Z025-90	Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART
13Z100-91	Linux FPGA update tool (MEN)

Software: VxWorks

10EM03-60	VxWorks BSP (MEN) for EM3, EM3A, EM8, EM8A, EK7, A14C and F13
13P010-60	VxWorks UART driver (MEN) for P10 and P11
13Z025-60	VxWorks native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART
13Z100-60	VxWorks FPGA update tool (MEN)

Software: QNX

10EM03-40	QNX BSP (MEN) for EM3, EM3A, EM8, EM8A, EK7, A14C and F13
13Z025-40	QNX native driver (MEN) for 16Z025_UART and 16Z125_UART
13Z100-40	QNX FPGA update tool (MEN)

Software: Firmware/BIOS

14EM03-00	MENMON (Firmware) for EM3, EM3A, EM8, EM8A, A14C and F13 (object code)

Documentation

20A014-00	A14C User Manual
20A014CER	A14C Errata
21APPN009	Application Note: 16Z025_UART and 16Z125_UART under Linux
21MENM-00	MENMON 2nd Edition User Manual
22Z025-ER	16Z025_UART Errata

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the A14C online data sheet under » www.men.de.

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